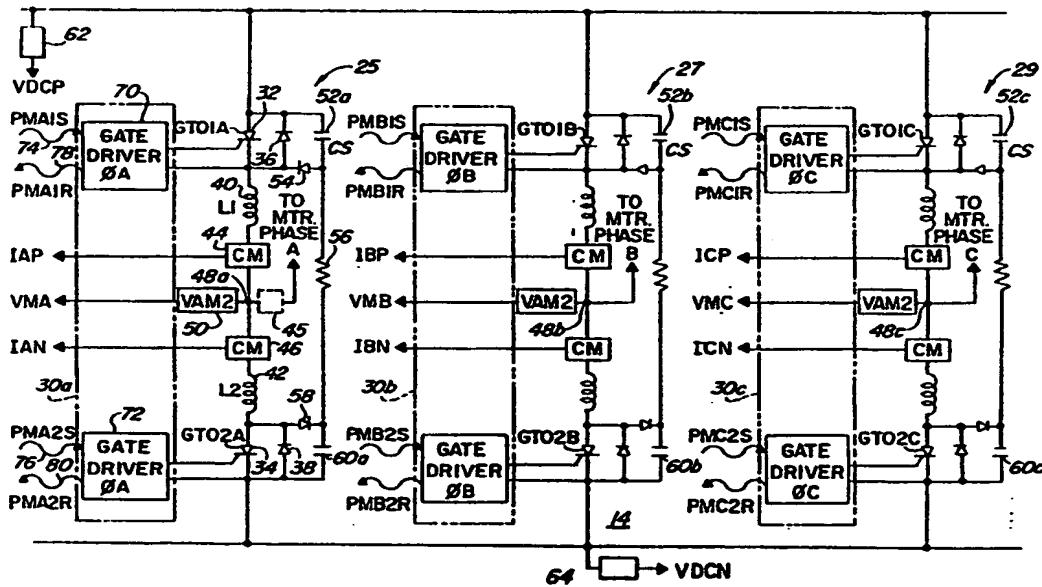




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(54) Title: AUTO-SELF TEST OF AC MOTOR SYSTEM



(57) Abstract

Apparatus and method for auto-self testing of a power converter and motor system wherein the power converter has three parallel legs, each including two series connected gate-turn-off thyristors (GTO) connected between a pair of DC power source buses. A microprocessor controls the test sequence in which each GTO is individually turned on in a predetermined order so as to create a transient snubber current through the motor and through each GTO when it is turned on. The snubber current and a voltage in each leg is measured and compared to a respective reference to detect wiring errors, and defects in the motor, the GTOs, and other system components. Error messages are generated in response to detection of abnormalities or defects.

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AUTO SELF TEST OF AC MOTOR SYSTEM

This Application is a continuation-in-part of U.S. Patent Application S.N. 07/630,681 filed December 20, 1990 and assigned to the assignee of the present invention.

5

BACKGROUND OF THE INVENTION

This invention relates generally to an apparatus and method for testing AC motor power systems and, more particularly, to an apparatus and method for nondestructive in-circuit testing for short-circuit conditions in an inverter power circuit.

It is common in AC electric motor drive systems to employ power inverter systems to furnish electric power from a DC source to an AC motor. These inverter systems are of various types, but are often comprised of gate turn-off thyristors (GTO) in a bridge arrangement. The GTOs in the bridge are selectively gated to control the electrical power supplied to the motor by converting DC power from the DC source into AC power which drives the motor. Typically, two GTOs are connected in a series arrangement in what is commonly referred to as a "leg" between relatively positive and relatively

negative busses of the DC source. A common converter of this type is a three-phase converter having three legs connected in mutual parallel between the positive and negative DC source busses.

5 The GTOs of each of the legs are rendered conductive in a predetermined order or sequence in order to control the electrical power delivered from the DC busses to the AC motor.

The above described motor systems require regular maintenance to avoid or detect a variety of common failure modes. For example, if both GTOs of a leg were to become conductive simultaneously, there would exist a short between the DC source busses which, if allowed to continue, could result in great damage to the motor, power source, and/or to the GTOs. In addition, failure of various components and segments of the system such as the feedback circuits, drive circuits, and the motor load itself can occur. In prior art, expensive and time consuming manual off-line testing has been necessary to detect many errors at an early enough stage to ensure proper operation. In order to enhance maintenance of such systems, it would accordingly be highly desirable to provide an auto self test capability and, in particular, to provide a test capability to identify short-circuit conditions prior to initiating operation of an inverter.

The above as well as other desirable features are achieved in accordance with the present invention by testing a power inverter prior to enabling inverter operation. In an illustrative form, the power inverter has a plurality of legs having first and second series connected controllable switching devices, such as GTOs,

connected between positive and negative DC voltage busses. The testing method includes measuring the voltage intermediate the switching devices prior to enabling the devices into conduction. The measured 5 voltage is then compared to the voltage at each of the voltage busses. If the measured voltage is substantially equal to either one of the bus voltages, one of the devices is short-circuited and the system is inhibited from initiating operation of 10 the inverter.

In a preferred form, the voltage intermediate the switching devices is measured a preselected time period after power is applied to the voltage busses, the time period being selected to be sufficiently 15 long to allow the voltage to settle and sufficiently short to prevent the voltage from discharging through the load or the measuring device.

SUMMARY OF THE INVENTION

In an illustrative form, the present invention 20 comprises a method for testing a power inverter in which the power inverter has at least one leg connected between relatively positive and relatively negative voltage busses. Each inverter leg has a first and a second series connected controllable 25 switching device and each device has a parallel connected capacitor. The method comprises the steps of sampling voltage at a junction intermediate the switching devices; comparing the sampled voltage to a voltages present on the voltage busses; and generating an indication of device failure in 30 response to a substantial equality between the sampled voltage and the voltage of either voltage bus. The step of sampling voltage may include measuring the voltage in a period of time

substantially less than a discharge time of the capacitors when discharging through a load coupled to the inverter. For a load comprising a three-phase motor, the inverter includes at least three 5 legs and the step of sampling includes the steps of sampling voltage in each leg for comparison to each bus voltage.

In one implementation, the invention is shown in combination with a power inverter system 10 including an inverter having at least three legs for providing three phases of output power with each leg including a pair of controllable switching devices serially coupled between relatively positive and relatively negative voltage busses. Each switching 15 device is coupled in parallel with a corresponding capacitor and each capacitor has a substantially identical capacitance. A junction intermediate each serially connected pair of switching devices is coupled to a respective power input terminal of a 20 three phase AC electric traction motor. A controller is operatively coupled to the inverter for providing signals for selectively switching the switching devices between conductive and non-conductive states. A voltage sensor is coupled to 25 each of the power input terminals for determining the voltage at each of the terminals prior to providing the switching signals. The voltage sensor is electrically coupled to the controller and the controller is responsive to the voltage sensor for 30 inhibiting starting of the switching signals when the sensed voltage is substantially equal to either of the voltages of the positive and negative voltage busses.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The invention, together with further objects and advantages thereof may be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a generalized block diagram illustrating an AC motor drive system;

FIG. 2 is a detailed block diagram of the power inverter circuit shown in FIG. 1;

10 FIG. 3 is a detailed block diagram of the control logic shown in FIG. 1;

15 FIGS. 4A and 4B are diagrammatic illustrations of the inverter circuit operation and time dependant plots of voltage and current during one form of auto self test:.

FIGS. 5A to 5D are detailed flow diagrams illustrating the methodology and structural flow of a specific embodiment of an auto test routine;

20 FIG. 6 are time dependent plots of voltage in the inverter at initial power on.

DETAILED DESCRIPTION

FIG. 1 is a block diagram of a specific embodiment of a three-phase, voltage source inverter driven motor system 10 with which the present invention may be used. System 10 is illustrated as including a three-phase AC motor 12 driven by a three-phase voltage source inverter 14 supplied by a DC power source 16. Although it will be recognized that the invention is applicable to a wide range of power converter-load configurations, for example, single phase converter and single phase motor; multiple motors in parallel driven by a single converter; transformer loads; and other inductive or resistive loads. Coupled to the

inverter 14 is a gate driver module 18 which is controlled by a control logic circuit 20. In operation, the inverter 14 converts the DC power from DC source 16 into a three-phase excitation voltage for application to respective phase windings A, B and C of motor 12 in response to gate drive signals from gate driver module 18. The gate driver module 18 controls the switching of the inverter switching devices (i.e., GTOs) in the inverter 14 and is in turn controlled by the control logic circuit 20 via an optical control link 19. In addition, feedback status signals from the GTO devices of the inverter 14 are coupled back to the gate driver module 18 and to the control logic circuit 20 via the optical link 19. Additional signals from current and voltage sensors of the inverter 14 are coupled to the control logic circuit 20 via a bus 21, as shown. The control logic circuit 20 uses the feedback values from the optical link 19 and the sensed current and voltage values via the bus 21 to perform the auto self test method in accordance with the invention. In a typical application, such as a commuter rail car, the inverter 14 may be configured to drive two motors in parallel and a single control circuit may control a total of four motors.

Referring now to FIG. 2, there is shown a detailed schematic diagram of a three-phase inverter 14 including gate driver circuits 18a, 18b, and 18c incorporating the teaching of the present invention. Such gate driver circuits 18 are described in detail in a co-pending patent application entitled "Gate Turn-off Thyristor Control Circuit with Shorted Gate Detector" filed by R.B. Bailey and H.J. Brown on September 18, 1990

bearing Serial Number 07/584,541 and assigned to General Electric Company which is hereby incorporated by reference. The inverter 14 comprises a first leg 25 (phase A) with an upper 5 GTO 32 and a lower GTO 34 arranged in series with the anode of the upper GTO 32 coupled to the positive DC source bus 33 and the cathode of the lower GTO 34 coupled to the negative DC source bus 35. The GTOs 32, 34 may typically be mounted on a 10 heat sink with a temperature sensing thermal resistor (not shown) mounted thereon to detect overheating.

For each GTO 32, 34, there is a respective anti-parallel diode 36, 38 connected from anode to cathode to provide a return path for inductive load currents. An upper inductor (L1) 40 (e.g., 5 μ h) and lower inductor (L2) 42 are coupled in series with the GTOs 32, 34. Also in series with the inductors L1, L2 are an upper current measurement 20 circuit 44 (e.g., a Model LT1000-FI/SP45 Manufactured by LEM of Switzerland) and a lower current measurement circuit 46 which are connected at a Phase A node 48, as shown. The node 48 is coupled to one phase (phase A) of the three-phase 25 motor (or motors) 12 and, as shown, to a conventional high impedance voltage measurement circuit 50. The current measurement circuits 44, 46 thus generate current measurement signals IAP and IAN to be coupled to the control logic circuit 20 30 via bus 21. The current measurement circuits may alternately be implemented with a single current measurement circuit 45 coupled in series between the node 48 and the motor phase A. The voltage measurement circuit 50 generates a voltage 35 measurement signal V_m which is coupled to the

control logic circuit 20.

A snubber circuit is also coupled to the phase A leg 25 and comprises a capacitor 52 and diode 54 coupled across the GTO 32 and a 5 capacitor 60 (e.g., $3\mu\text{f}$) and diode 58 coupled across the GTO 34, as shown. A resistor 56 (e.g., .25 ohms) provides a discharge path for the snubber capacitors 52, 60. Conventional high impedance voltage measurement circuits 62, 64 are coupled 10 respectively to the positive DC voltage source bus 33 and negative DC voltage source bus 35 to provide a positive voltage source measurement signal VDCP and a negative voltage source measurement signal VDCN.

15 The gate driver circuit 18a comprises an upper gate driver 70 and a lower gate driver 72, each of which is coupled to the gate and cathode of the respective GTO 32, 34, as shown. The gate drivers 70, 72 provide drive signals to the gates of 20 the GTOs 32, 34 to turn them on and off at the proper time. The gate drivers 70, 72 also detect whether the GTO actually did turn on or off in response to the signal (i.e., gate status feedback). In addition, each gate driver 70, 72 is coupled to 25 the control logic circuit 20 via conventional optical couplers to permit input of gate command signals (PMA1S, PMA2S) from the control logic circuit 20 on respective input channels 74, 76, and to send gate status feedback signals (PMA1R, PMA2R), indicating whether the GTO is turned on or 30 off, back to the control logic circuit 20 on respective transmit channels 78, 80.

35 The inverter power circuit 14 of FIG. 2 further comprises two additional legs 27, 29 (i.e., phase B, phase C), which are substantially identical to

phase A leg 25, as shown. The phase B leg 27 is connected to the AC motor phase B and the phase C leg 29 is connected to the AC motor phase C while the input and output optical lines and 5 measurement signals are coupled to the control logic circuit 20 as described with regard to the phase A leg 25.

FIG. 3 is a detailed block diagram of the control logic circuit 20 of FIG. 1, and comprises 10 three main blocks: an input module 98, a processor module 100 and an output module 102. A detailed description of such a control logic circuit is provided in co-pending application entitled "Inverter Control Method and Apparatus" filed by 15 A.K. Kumar and T.D. Stitt on November 27, 1990 bearing Serial No. 07/618,787 and assigned to General Electric Company, which is hereby incorporated by reference. The input module comprises a conventional summing circuit 104 for 20 phase A, a conventional summing circuit 106 for phase B, and an optional conventional summing circuit 108 for Phase C, each of which combines the respective upper and lower current measurement values to obtain a motor phase current value for the 25 corresponding phase (i.e., IMTRA, IMTRB, IMTRC). Since IMTRC can be derived as the sum of the currents of phases A and B, summing circuit 108 is optional. In addition, if the optional single 30 current measurement circuit 45 in the inverter 14 of FIG. 2 is used for each phase, no summing circuits are needed. In each case, the motor phase current value is coupled from the input module 98 to analog to digital (A/D) converters 110, 112 (e.g., high speed, 10 bit A/D converter such as model ADC856 35 manufactured and marketed by Datel of Mansfield,

Mass.) and optionally, to an A/D converter 114 in the output module 102. The A/D converters 110, 112, 114 convert the motor phase current values to digital form and couple them through a standard cell 116 (such as that described in the RCA Solid State Data Book SC 3001.5 Micron Standard Cells, copyright 1987 by RCA Corp.) to a processor 120 via a bus 122, as shown. Alternatively, the digitized signals can be coupled directly to the processor 120 from the A/D converters.

The input module also couples the voltage measurement values V_{m1} , V_{m2} , V_{m3} from the inverter 14 to respective summing circuits 124, 126, 128, along with the negative DC source voltage measurement signal VDCM, as shown. These summing circuits thus provide voltage measurement values (V_A , V_B , V_C) referenced to negative DC source bus 35 which are coupled to a converter circuit 130. The converter circuit 130 converts the signals from three-phase signals (V_A , V_B , V_C) to two-phase signals (V_B , V_Q , V_{MS}) which are coupled to an A/D converter 132 (e.g., a high speed, 12 bit A/D converter, model ADC80, manufactured by Analog Devices located in Norwood, Mass.) of the processor module 100, as shown. Alternatively, V_A , V_B , V_C values may be coupled directly to the A/D converter 132. The A/D converter 132 converts the input values of V_A , V_B , and V_C to digital form and couples the digitized values to a processor 120 via a bus 134. The positive DC voltage bus measurement value VDCP from the inverter 14 is also coupled to the input module 98 and is coupled to a summing circuit 136 along with the negative DC voltage bus value VDCN. The summing circuit 136 generates a voltage difference signal V_L , representing the actual voltage

source line voltage, which is also coupled to the A/D converter 132. The A/D converter 132 digitizes the value of V_L and couples the digitized value to the processor 120, as shown.

5 The processor 120 of the processor module 100 may be a single microprocessor (e.g., a model 80960CA such as that manufactured by Intel of Santa Clara, California) or it may be a dual processor structure, such as illustrated, comprising an X 10 processor 140 and a Y processor 142 (e.g., an Intel 80186 manufactured and marketed by Intel Corporation of Santa Clara, California) both coupled to a dual port random access memory (RAM) 144 (e.g., models IDT7130 and IDT 7140 such as manufactured by 15 Integrated Devices Technology of Santa Clara, California). The processor 120 outputs signals via the bus 122 to the standard cell 116 of the output module 102 and communicates with external devices such as an external processor or a display (e.g. for 20 error messages, etc.) via a serial link 141. In addition, inputs from a port 146 are coupled to the processor 120 from the output card 102. The processor 120 is controlled by a program stored in each PROM 145, 147 to process the input values from 25 both the output module 102 and the input module 98 and generate output control signals coupled on the bus 122 to the standard cell 116 to control the auto self test of the inverter-controlled motor system 10.

30 The output module 102 includes a conventional optical receiver circuit 150 (e.g., model HFBR2522, manufactured and marketed by Hewlett Packard of Palo Alto, California) which receives the optical GTO 35 status feedback signals (PMA1R, etc.) from the inverter driver module 18, and couples them in

electrical form to a logic buffer circuit 160 via a bus 152. These signals are also coupled to the processor 120 via the port 146, as shown. In addition, gate firing pulses from the standard cell 116 are coupled to the logic buffer circuit 160 via a bus 154. The logic circuit 160 couples gate pulses (i.e., gate "on" or "off" command signals) to an optical driver 162 (e.g., model HFBR1521, marketed and manufactured by Hewlett Packard of Palo Alto, California) which generates optical gate command signals (PMA1S, etc.) which are coupled via the optical channel to the inverter 14. In addition, the gate command signals from the logic buffer circuit 160 are coupled via a bus 164 to the processor 120 via the port 146, as shown.

In normal operation, the control logic circuit 20 generates gate command signals which are coupled to the gate driver module 18. The microprocessor 120 of the module 100 controls generation of gate firing pulses by providing gate firing control signals to the standard cell 116 via the bus 122. The standard cell 116 generates gate firing control pulses in response to the gate firing control signals from the microprocessor 120. These gate firing control pulses are coupled to the logic buffer 160 via the bus 164 which couples gate command signals to the optical driver 162 for transmission to the gate driver module 18. The GTOs of the inverter 14 are then turned on and off by the gate driver module 18 at the appropriate times under the control of the gate command signals. Additionally, gate status feedback signals received from the optical receiver 150 are coupled to the logic buffer 160 which utilizes them to determine if the GTOs actually switched, as commanded, in order

to prevent unwanted conditions such as having both upper and lower GTOs turned on at the same time.

During the auto self test, the motors are stopped and the GTOs are turned on and off under control of the processor 120 using the method according to the invention. The processor then analyzes the voltages and currents measured during the test sequence and generates appropriate error messages if an abnormality is detected.

FIGs. 5A-5D are detailed block diagrams illustrating a specific embodiment of a program logic for the microprocessor 120 and the methodology of the auto test according to the invention. FIGs. 4A-4B illustrate the operation of the inverter tests and the associated voltages on current versus time plots, and may be referred to in conjunction with FIGs. 5A-5D to appreciate the invention.

Referring to FIG. 5A, the test routine is entered at block 300, as shown, and begins with the turnoff of all GTOs, as illustrated by block 302. Off commands are sent to all six GTOs (See FIG. 2) and those commands are verified to be off by checking the gate command signals which are output from the logic buffer 160 and fed back to the processor 120 via the port 146, as shown at FIG. 3. The currents through both phase A and B are then checked after a short delay (e.g., 1 millisecond) to determine if they are zero, as illustrated by block 304. The current check is performed by checking the values of IMTRA, and IMTRB which have been digitized in the A/D converters 110, 112, and coupled to the processor 120. A small delay (e.g., 100 microseconds) after the current check, the gate status feedback signals coupled through the optical receiver 150 are checked to verify that all GTOs are

off.

If any of the tests at blocks 302, 304 or 306 result in detection of an abnormality, an error message is generated, the fault flag is set and the 5 test proceeds normally, as illustrated by blocks 308, 310 and 312. The error message is passed from the processor 120 to an external display or other output device via the serial link 141. If a fault occurs, the test sequence will continue 10 normally for that GTO sequence. However, all subsequent test sequences of other GTO's will not be performed. Thus, at block 313, the fault flag is checked and if set, processing control branches to the end of the test routine skipping all subsequent 15 test sequences. If the fault flag is not set, processing continues to block 314 as shown.

An initializing sequence to initialize the inverter circuit 14 for the auto self test begins if no fault was detected with the turn-on of the lower 20 A phase GTO 34 by generation of a turn-on command for the A phase GTO, as illustrated by block 314. The on command and the off commands for all other GTOs are verified, as illustrated by block 316, by checking the output command signals to the optical 25 drive 162. This turn-on of the lower A phase GTO results in the voltages V_A , V_B , and V_C (i.e., the voltages at nodes 48, 48b, and 48c) dropping to zero by means of discharge of the snubber capacitors 60b and 60c through the phase B and phase C and then 30 through phase A motor coils to the DC source line through the turned-on GTO 34. The node voltages V_A , V_B , and V_C are then checked by the processor and verified to be low (i.e., approximately zero) after 35 allowing enough time to permit discharge of the snubber capacitors 60b and 60c and the charging of

the snubber capacitors 52a, 52b and 52c, as shown by block 318. The gate status feedback signal for the lower A phase GTO 34 is then checked to determine if it is on and all other gate status feedback signals 5 are checked to determine if they are off, as illustrated by blocks 320 and 322 (see FIG. 5B). The lower A phase GTO 34 is then turned off (i.e., an off command is generated) as illustrated by block 324 of FIG. 5B and its gate status feedback 10 signal is checked to verify that the GTO 34 is off as shown by block 326. If any of the tests at blocks 316, 318, 320, 322, or 326 are negative, an error message is generated, the fault flag is set, and the test sequence then proceeds to the next 15 step, as illustrated by blocks 328, 330, 332, 334, and 336. Processing continues normally until the next fault flag text at block 338 where processing control branches to the end if the fault flag is set.

20 The main test sequence of the auto self test routine begins at block 340, if no fault was detected, with turn-on of the upper A phase GTO 32. The phase A, B, and C nodes 48, 48b, 48c were made zero volts by turning on the lower A phase GTO 34 25 during initialization (see block 314). Referring to FIG. 4A, when the A phase upper GTO 32 is turned on, the A phase voltage V_A is pulled to the DC positive bus voltage and the snubber current through the phase B and phase C snubber capacitors flows through 30 the phase A node 48 as the phase B and phase C voltages V_B and V_C charge up to the DC positive bus voltage. This results in the voltage versus time plots illustrated in FIG. 4A for V_A , V_B , and V_C and current versus time plots for I_A , I_B , and I_C . After 35 the on command is generated for the upper A phase

GTO 32, the on command signals and all the other GTO off command signals are checked to determine if they are correct, as illustrated by block 342. The current through phase A is then checked as illustrated by block 344 by rapidly sampling it during a period from zero to 300 microseconds after the command is generated, and obtaining the peak current value (I_{pk}). The peak current may also be obtained by waiting a predetermined time after the on command is generated and measuring the current at that time to obtain a peak current. The peak current obtained is compared to a reference value to determine if it is substantially equal to the reference value, as shown by block 346. In one embodiment, the reference value is given by the relationship $V_L \cdot (C/L)^{1/2}$ where V_L is the line voltage (e.g., DC+), C is the equivalent capacitance of the total circuit snubber capacitance, and L is the equivalent motor inductance. The phase A, B and C voltages (V_A , V_B , V_C) are then verified to be high (i.e., near the positive DC source bus voltage) as illustrated by block 348. The gate status feedback signals are then checked to determine if the upper A phase GTO 32 is turned on and if all the other GTOs are off as shown by block 350 (see FIG. 5C). The upper A phase GTO 32 is then turned off by generating an off command signal as illustrated by block 352 of FIG. 5C and the gate status feedback signal is checked to verify that it is off, as illustrated by block 354. If there are any abnormalities indicated by a negative result at blocks 342, 346, 348, 350; or 354, an error message is generated, the fault flag is set, and the test sequence proceeds to the next step, as illustrated by blocks 356, 358, 360, 362, or 364. Processing

continues until the fault flag test at block 368 where processing control branches to the end if the fault flag is set.

The next sequence of the auto self test begins, 5 if no fault was previously detected, with the turn-on of the lower A phase GTO 34 by generation of an on command as illustrated by block 370. Referring to FIG. 4B, the phase A, phase B and phase C nodes 48, 48b, 48c were previously pulled to the 10 positive DC bus voltage by the previous turn-on of the upper GTO 32. Thus, when the lower A phase GTO 34 is turned on, pulling node 48 to the negative DC bus voltage, the snubber current from the 15 discharge of the phase A and phase C snubber capacitors flows through the phase A node 48 until the phase B and phase C nodes 48b and 48c are discharged to the negative DC bus voltage. This results in the voltage versus time characteristics 20 for V_A , V_B , and V_C and for the current values I_A , I_B , and I_C , as illustrated in FIG. 4B. The gate on command for the lower A phase GTO 34 and off commands for all other GTOs are verified by checking 25 the command signals, as shown by block 372. At blocks 374 and 376, the peak discharge current is then measured and checked against the reference, as described with regard to the previous sequence at 30 blocks 344, 346. The three-phase voltages V_A , V_B , and V_C are then sampled and verified to be low (i.e., approximately at the negative DC line voltage) as 35 illustrated by block 378. The gate status feedback signals of all GTOs are then checked to verify that the lower A phase GTO 34 is on and all others are off as shown by block 380 (see FIG. 5D). The lower A phase GTO 34 off command is generated to turn off the GTO 34 and the gate status feedback for the

GTO 34 is checked to be off as illustrated by blocks 382 and 384 of FIG. 5D. If the result of any of the tests at blocks 372, 376, 378, 380, or 384 are negative, an error message is generated, the
5 fault flag is set, and the test sequence then proceeds normally as illustrated by blocks 386, 388, 390, 392, or 394. Processing then continues normally until the next fault flag test at block 398 where processing control branches to the end if the
10 fault flag is set.

The test sequence next performs the test of phase B, if no fault was previously detected, with the upper B phase GTO turned on, as illustrated by block 400. This test sequence uses the same
15 sequence as the phase A testing sequence for the top A phase GTO 32 turn-on, as illustrated by blocks 340 to 364. Thus, block 400 represents the same test sequence as blocks 340 to 364 with the exception that it is the upper B phase GTO on command that is
20 generated and checked, and the I_B (IMTRB) peak current made up of phase A and phase C snubber discharge currents which is measured and checked. Similarly, the test sequence is completed when the
25 upper B phase GTO is turned off and the feedback is checked, as illustrated by block 402, after which the fault flag is checked at block 403 and, if set, program control branches to the end.

The next test sequence is performed, if no fault was detected, by turning the lower B phase GTO on, as illustrated by block 404. The test sequence represented by block 404 is the same as the test sequence for the lower A phase GTO turn-on test sequence illustrated by blocks 370-394, except that it is the lower B Phase GTO on command that is
35 generated and checked, and it is the I_B (IMTRB) peak

current which is measured and checked. The test sequence for the lower B phase GTO is completed by turning off the lower B phase GTO and verifying the turn-off by checking the status feedback for the 5 lower B phase GTO, as illustrated by block 406. The fault flag is then checked at block 407 and, if set, program control branches to the end of the routine.

An upper C phase GTO turn-on test sequence is next performed, if no fault was previously detected, 10 as illustrated by block 408 using the same test sequence as that described for the turn-on of the upper A phase GTO 32 described at blocks 340 to 364. This test sequence varies from that for the upper A phase and upper B phase GTO turn-on test in that 15 it is the upper C phase GTO on command that is generated and checked and it is I_c (IMTRC) or the sum of I_B (IMTRB) and I_A (IMTRA) peak current which is measured and checked. The upper C phase GTO on test is terminated by turning off the GTO and verifying 20 that it is off by checking the status feedback signal, as illustrated at block 410. The fault flag is then checked at block 411 and, if set, program control branches to the end of the routine. Next, 25 the lower C phase GTO turn-on test sequence is performed if no fault was detected, as illustrated at block 412, which is substantially the same sequence as described for the lower A phase GTO as 30 illustrated at blocks 370 to 394. The test sequence of block 412 differs from the test sequence for the lower A phase GTO 34 in that it is the lower C phase GTO on command that is generated and checked and it 35 is the I_c (IMTRC) or the sum of I_A (IMTRA) and I_B (IMTRB) peak current values which are measured and checked. The test sequence is ended by turning off the lower C phase GTO and verifying the status

feedback signal to ensure that the GTO is turned off. The test sequence is thus completed, as illustrated by block 416.

The system described thus far is useful in verifying operation of the GTO devices. However, another type of fault which may occur in a power inverter is a short-circuit condition which may exist prior to application of power or gating signals to the switching devices. If a short-circuit condition exists at the time power is applied to the inverter, subsequent gating of one of the switching devices into conduction may connect that device essentially between the positive and negative power busses and result in device destruction. Such a short-circuit condition may be caused through failure of a GTO or diode or an insulation breakdown in electrical cabling or in the motor load.

The present invention adds further testing which is performed prior to the above described testing to avoid a potential short-circuit problem in the power inverter circuit of FIG. 2 by applying voltage to voltage busses 33 and 35 with all the GTO devices 32, 34 turned off in each phase 25, 27 and 29. With the devices turned off, the voltage at each point 48a, 48b, 48c should be approximately one-half the value of the voltage between the busses 33, 35, assuming the snubber capacitors C_s (52,60) are of equal value. The voltage at 48 is read by the CPU 100 from the voltage measuring modules (VAMs) 50. The CPU 100 reads this voltage before the loading on points 48, due either to the VAMs or to leakage paths through the load, can discharge the voltage at the phases. Further, the voltage is desirably read after the capacitors C_s have had time

to charge so as to avoid questionable readings during charging.

5 If any one of the phases, i.e., points 48, is shorted to ground, i.e., bus 35, the voltage at that point 48 will be approximately zero volts (or such other voltage as is present on bus 35). Similarly, if any point 48 is shorted to bus 33, the voltage at point 48 will be approximately the voltage at bus 33.

10 Referring to FIG. 6, there are shown graphs of the voltage V_{dc} on the bus 33 and the voltages V_A , V_B , V_C at each point 48 of each phase of the inverter of FIG. 2. The initial time period indicated at T_c represents the charge time of the system as voltage is applied. The time indicated at T_u represents a valid measurement time interval, i.e., a time interval during which the voltage at point 48 should be approximately one-half the voltage V_{dc} . The voltage at points 48 continues to drop after the 15 interval T_u due to loading of the measurement devices 50 and the loads, e.g., motor 12. Thus, if the voltage at points 48 during time interval T_u is equal to about one-half V_{dc} , the inverter does not exhibit a short-circuit and the above described testing of 20 device operation can begin.

25

30 A program for implementing the initial short-circuit test is easily implemented in CPU 100 and requires only a timing function beginning with application of power to busses 33, 35 and a time-out occurring during interval T_u , followed by comparison of each measured voltage from VAMs 50 to a predetermined $\frac{1}{2} V_{dc}$ reference. A difference greater than a preselected maximum absolute value would indicate a shorted condition and be used to inhibit 35 inverter operation. Alternately, the measured

voltage at points 48 may be compared to the voltage at each bus 33, 35 and a failure indicated if the measured voltage is substantially equal to either bus voltage.

5 Specific embodiments of the novel method and apparatus for auto self test of an AC motor system have been described for the purpose of illustrating the manner in which the invention may be made and used. It should be understood that implementation
10 of other variations and modifications of the invention in its various aspects will be apparent to those skilled in the art and that the invention is not limited by specific embodiments described. It
15 is therefore contemplated to cover by the present invention any and all modifications, variations or equivalents that fall within the true spirit and scope of the underlying principals disclosed and claimed herein.

CLAIMS**WHAT IS CLAIMED IS:**

1. A method for testing a power inverter, said power inverter having at least one leg connected between relatively positive and relatively negative voltage busses, each leg having a first and 5 second series connected controllable switching device, each device having a parallel connected capacitor, the method comprising the steps of:

sampling voltage at a junction intermediate the switching devices;

10 comparing the sampled voltage to a voltages present on the voltage busses;

generating an indication of device failure in response to a substantial equality between the sampled voltage and the voltage of either voltage 15 bus.

2. The method of claim 1 wherein the step of sampling voltage includes the further step of measuring the voltage in a period of time substantially less than a discharge time of the 5 capacitors when discharging through a load coupled to the inverter.

3. The method of claim 2 wherein the load is a three-phase motor and the inverter includes at least three legs, the step of sampling including the steps of sampling voltage in each leg for comparison 5 to each bus voltage.

4. A power inverter system including an inverter having at least three legs for providing three phases of output power, each leg including a pair of controllable switching devices serially coupled between relatively positive and relatively negative voltage busses, each switching device being coupled in parallel with a corresponding capacitor and each capacitor having a substantially identical capacitance, each junction intermediate each serially connected pair of switching devices being coupled to a respective power input terminal of a three phase AC electric traction motor, control means operatively coupled to the inverter for providing signals for selectively switching the switching devices between conductive and non-conductive states, voltage measuring means coupled to each of the power input terminals for determining the voltage at each of the terminals prior to providing the switching signals, the voltage measuring means being electrically coupled to the control means and the control means being responsive to the voltage measuring means for inhibiting starting of the switching signals when the determined voltage is substantially equal to either of the voltages of the positive and negative voltage busses.

5. A method of pre-operation testing for a short-circuit condition in an electric power inverter having a plurality of phase legs connected in parallel circuit arrangement between a pair of relatively positive and relatively negative voltage busses, each of the legs including at least one pair of serially connected gate turn-off devices, each of the devices being connected in parallel with a

corresponding snubber capacitor, the method
10 comprising the steps of:

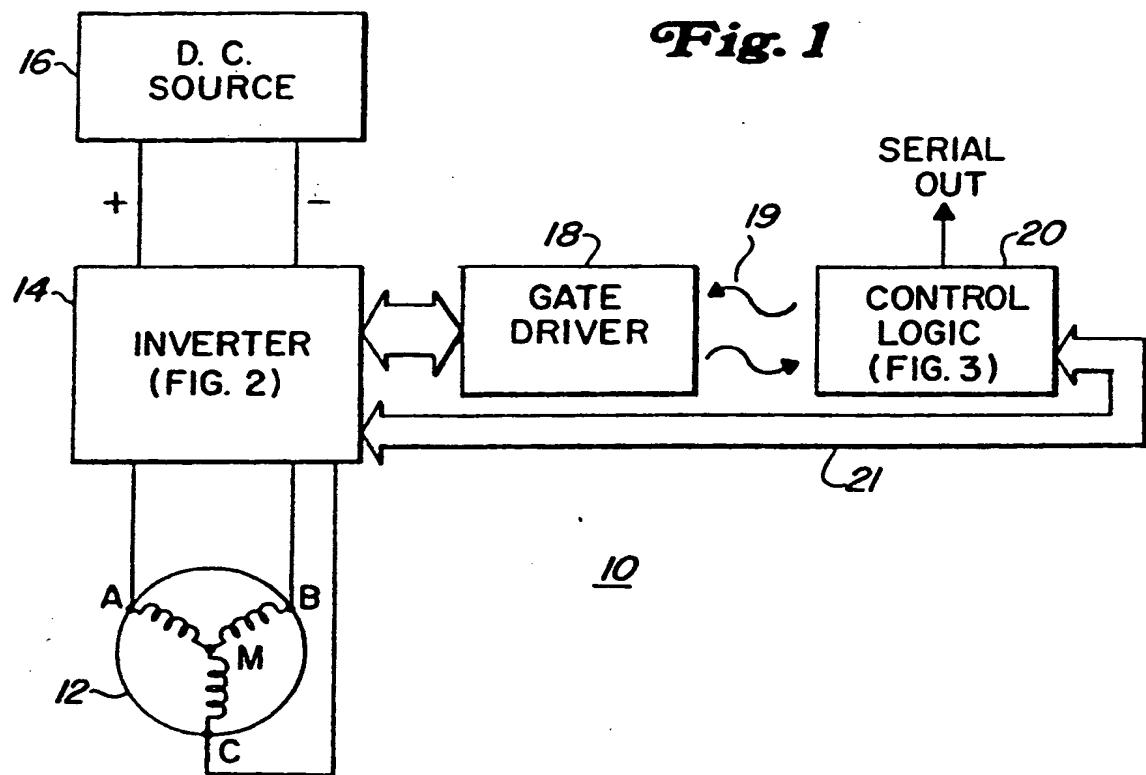
applying direct current electric power to the
voltage busses;

15 waiting a first predetermined time interval
selected to allow a voltage intermediate each of the
pair of devices to reach a maximum normal voltage;

measuring the voltage intermediate the devices
20 after the first predetermined time interval and
before expiration of a second predetermined time
interval selected to preclude normal discharge the
voltage;

comparing the measured voltage to a preselected
reference voltage approximately equal to the maximum
normal voltage for developing a voltage difference;
and

25 inhibiting operation of the inverter if the
step of comparing produces a voltage difference
greater than a predetermined value.



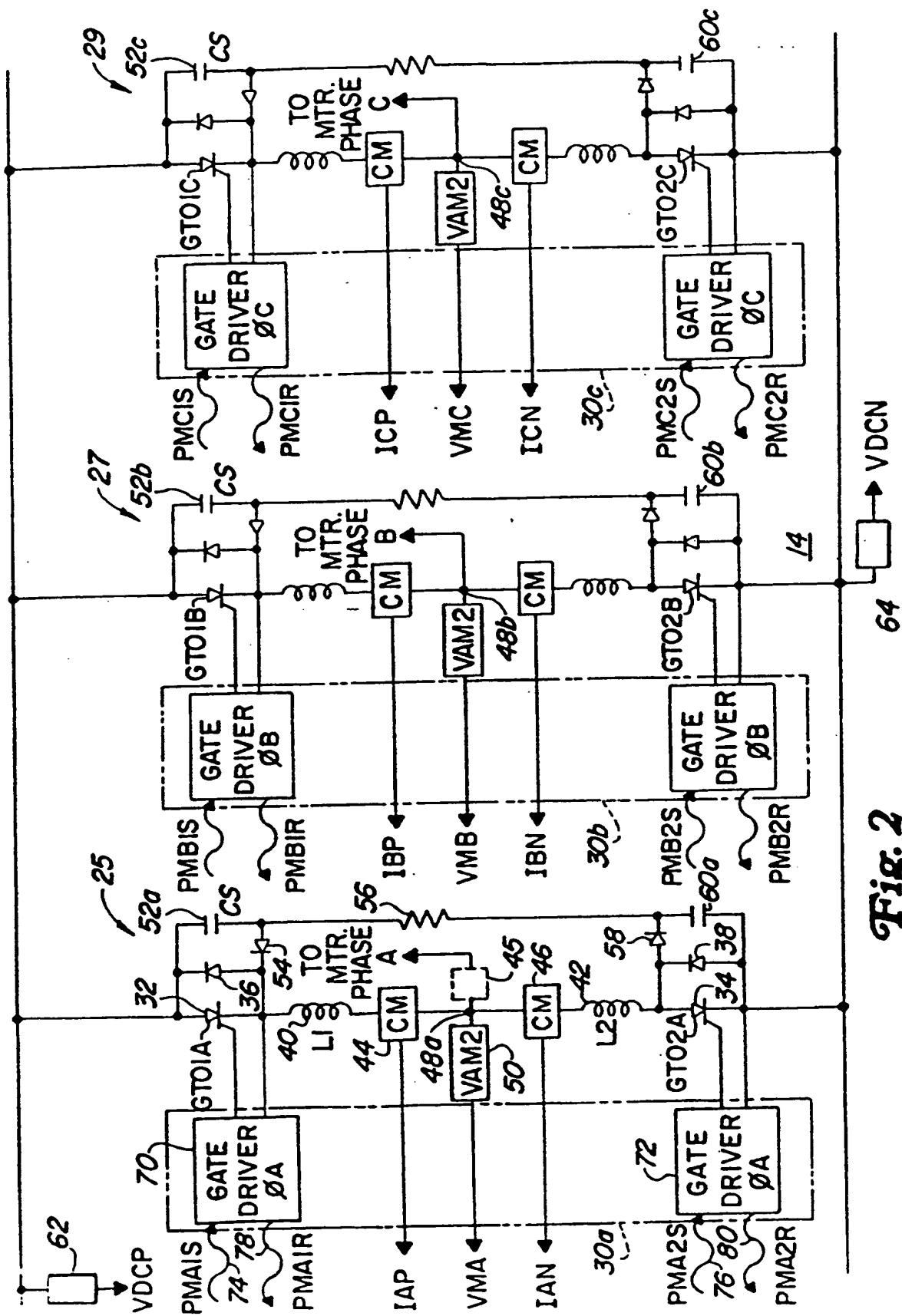


Fig. 2
64 → VDCN

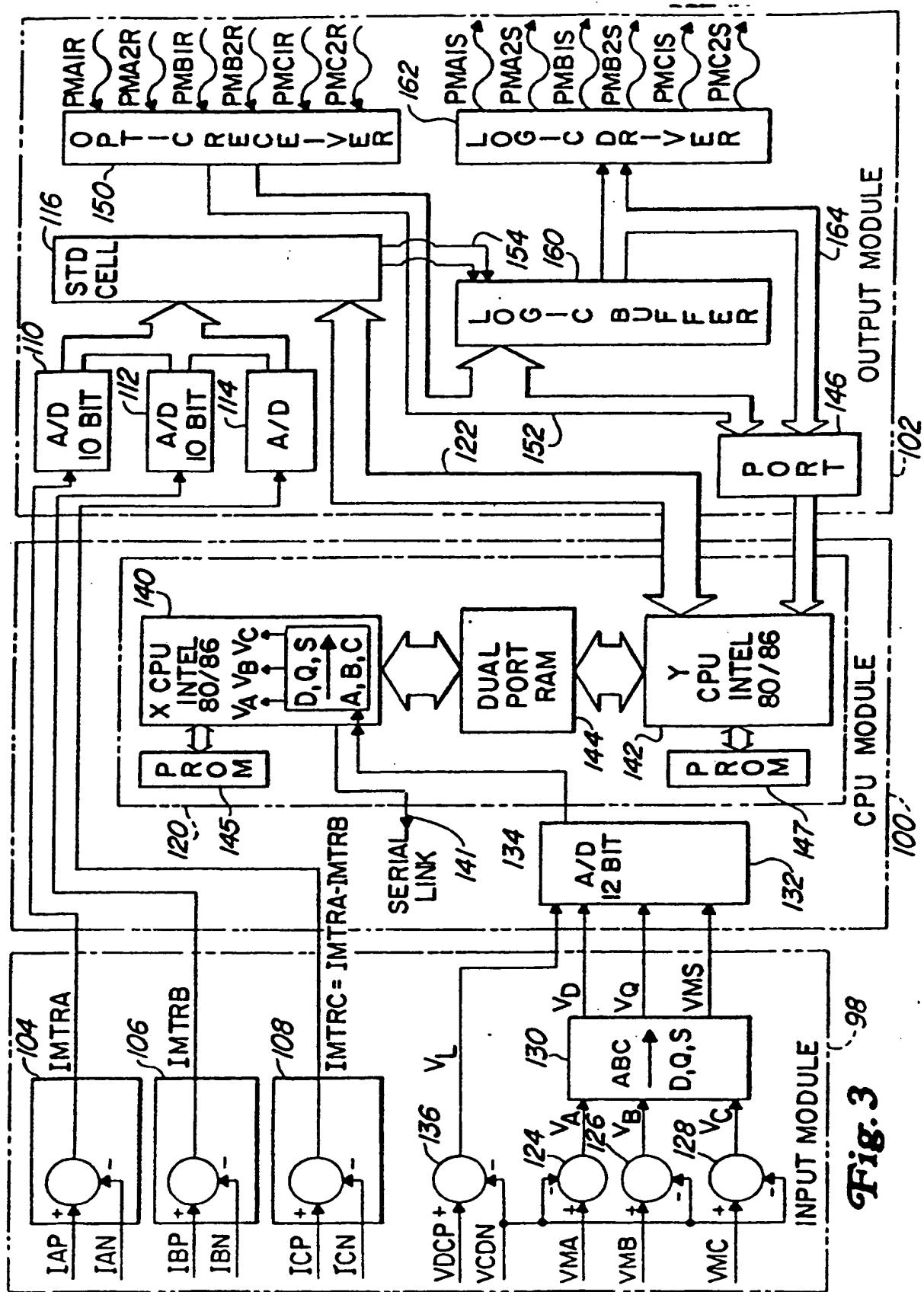
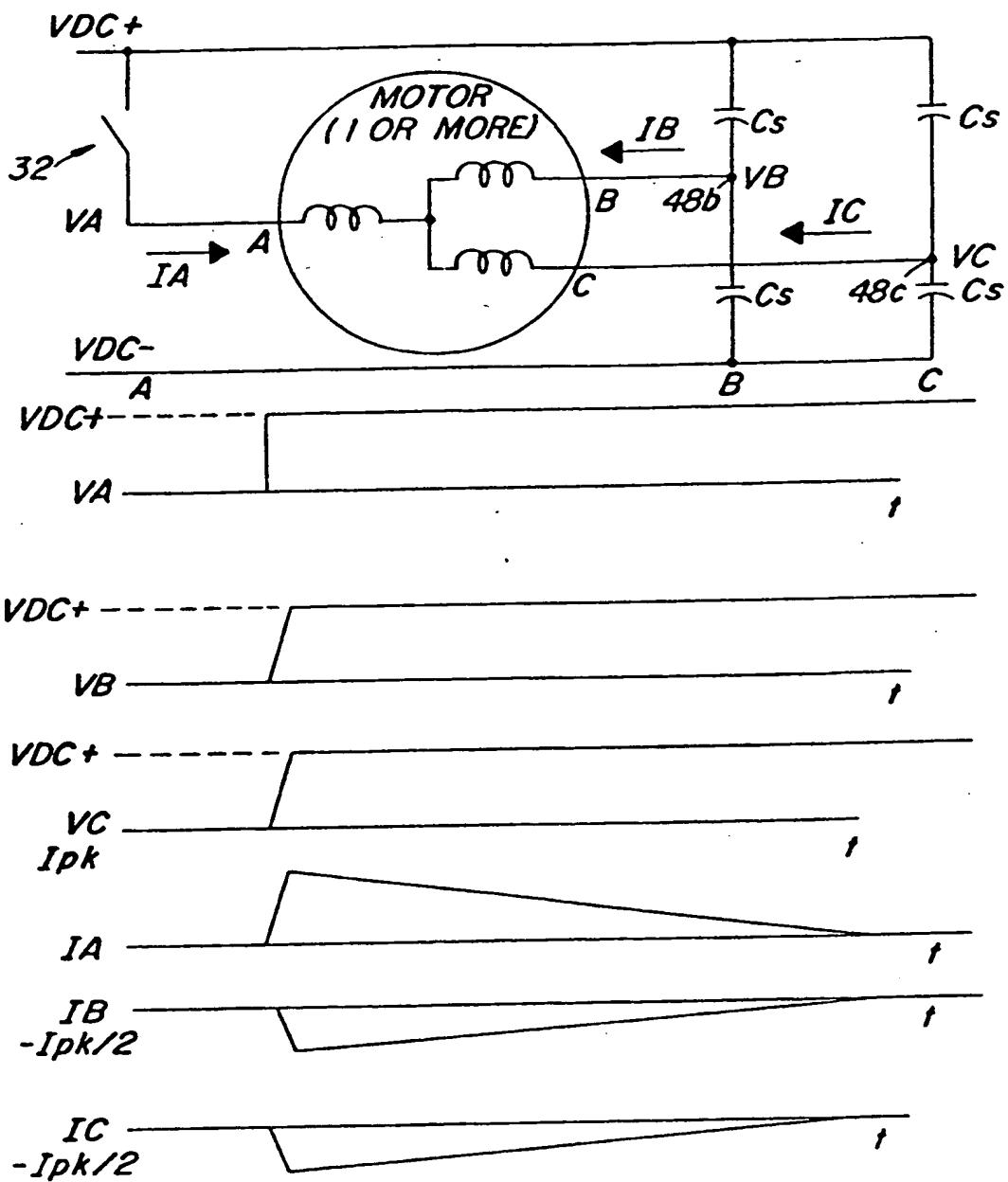


Fig. 3 - 98

**Fig. 4a**

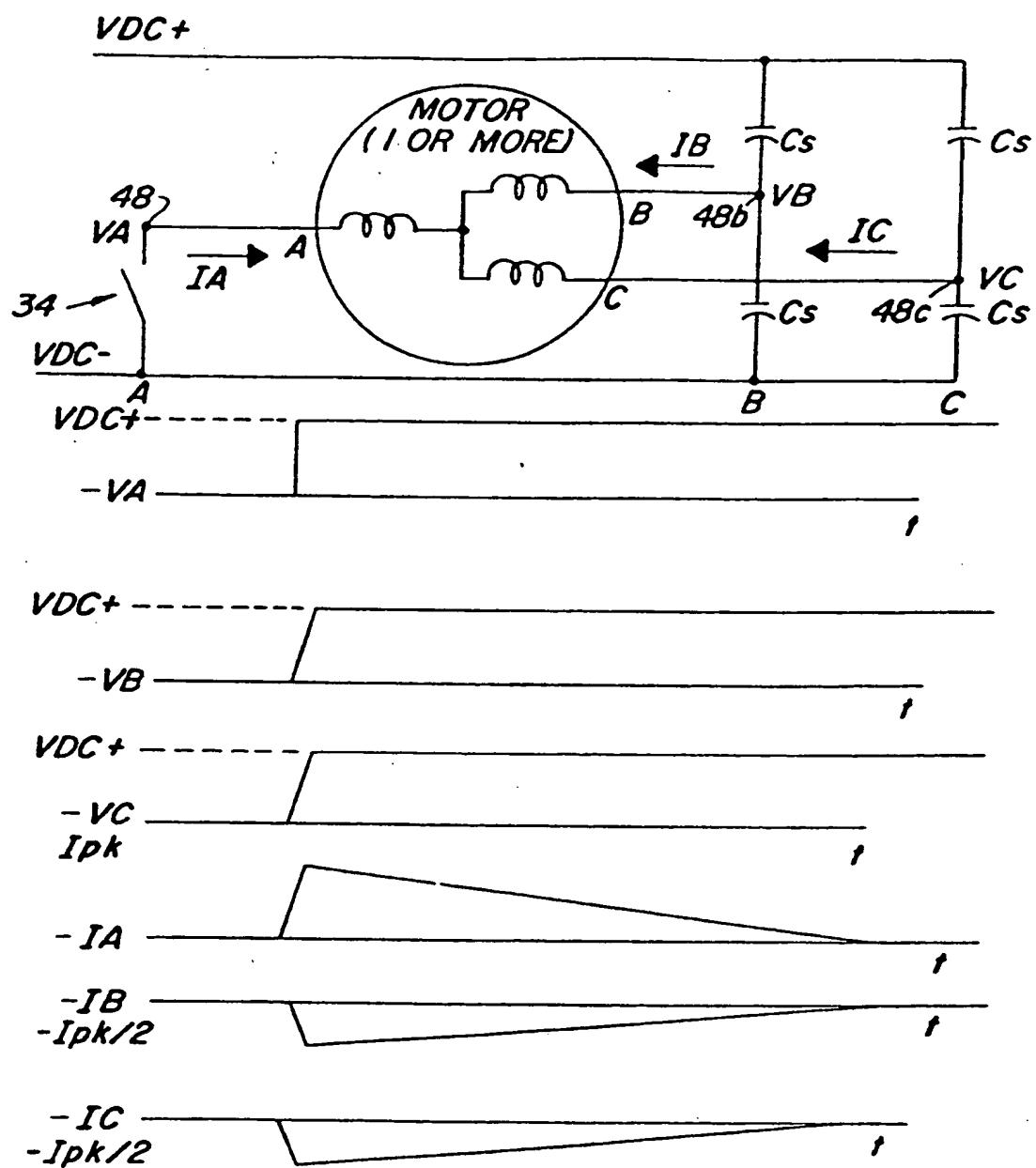


Fig. 4b

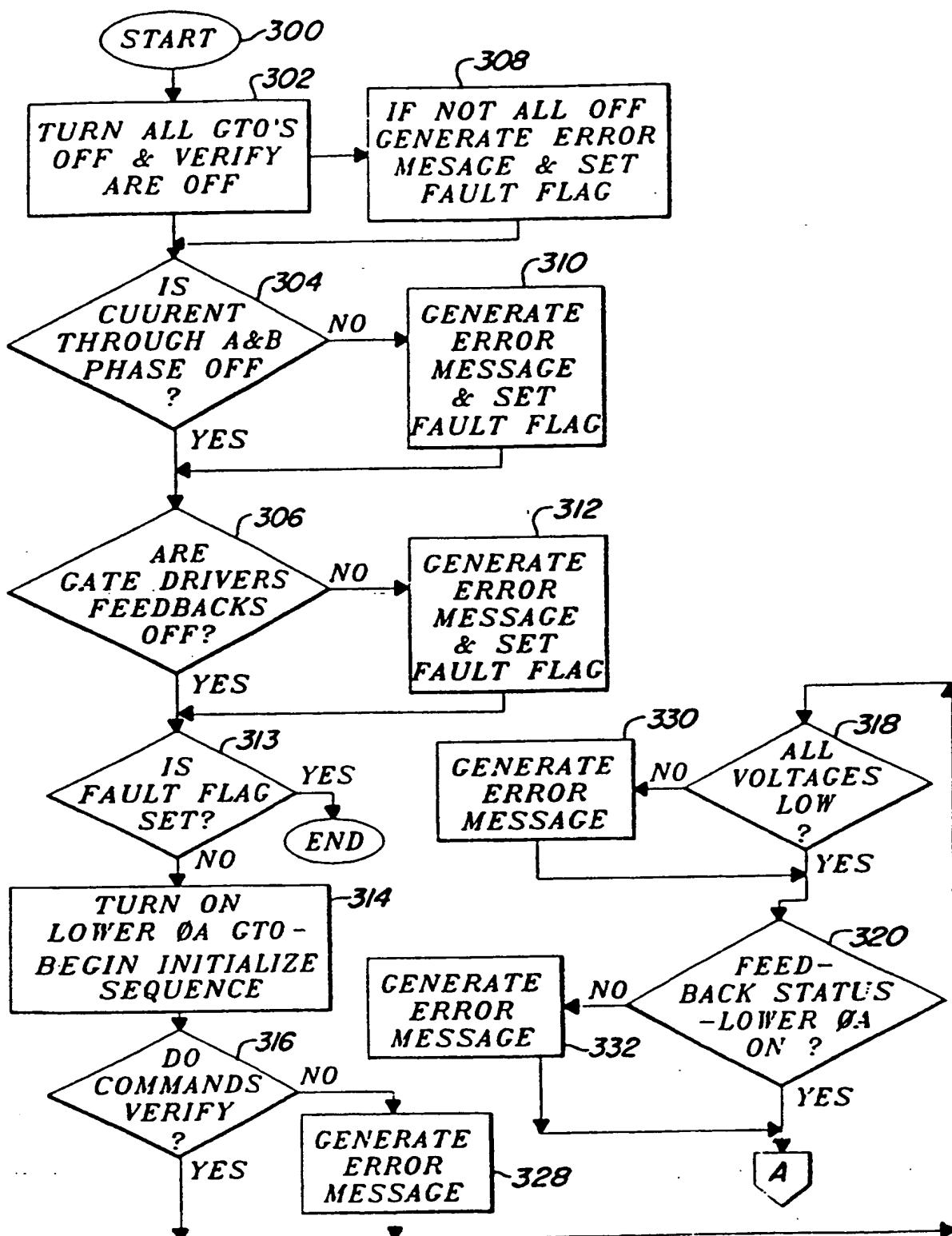


Fig. 5a

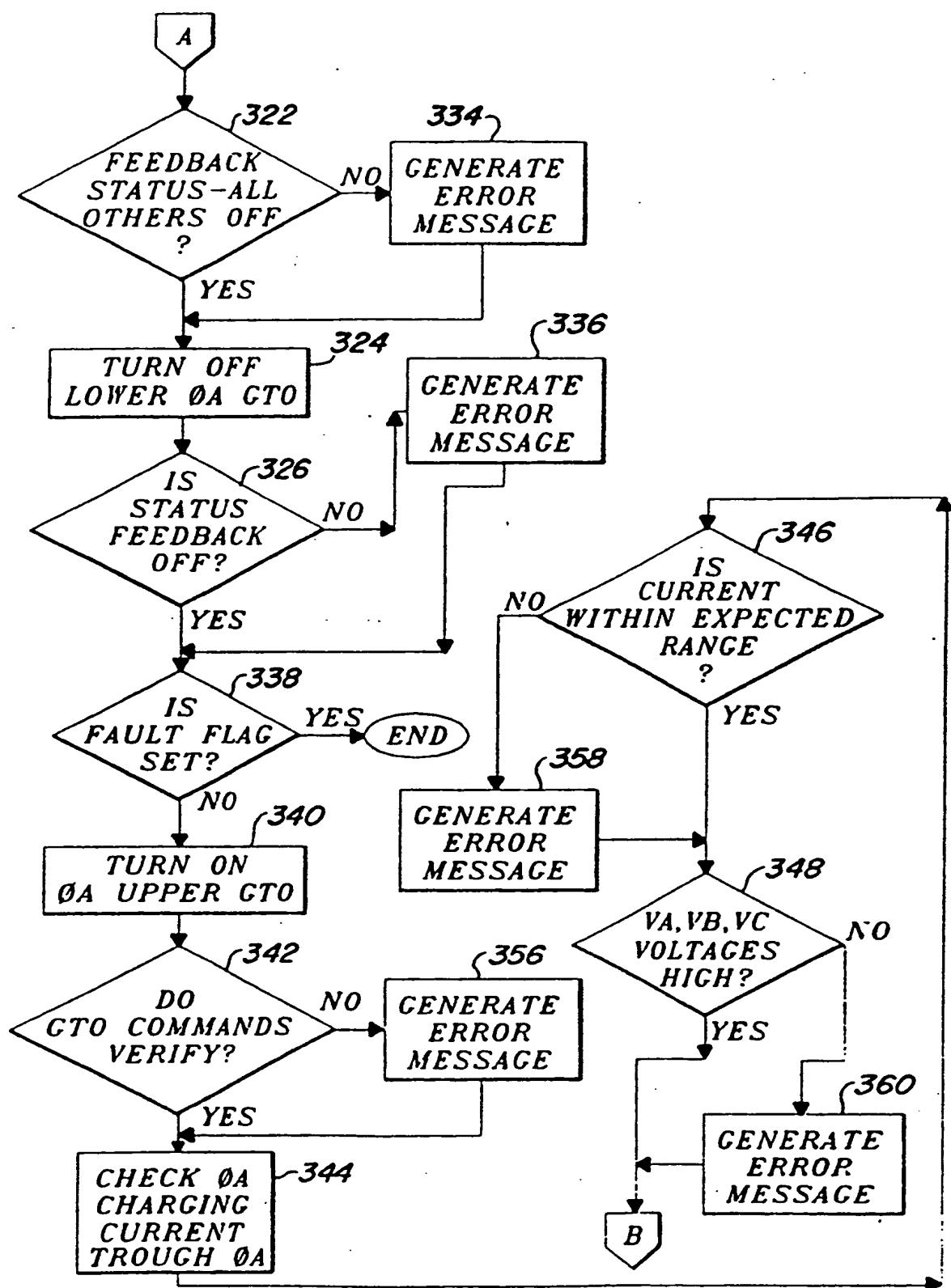


Fig. 5b

SUBSTITUTE SHEET

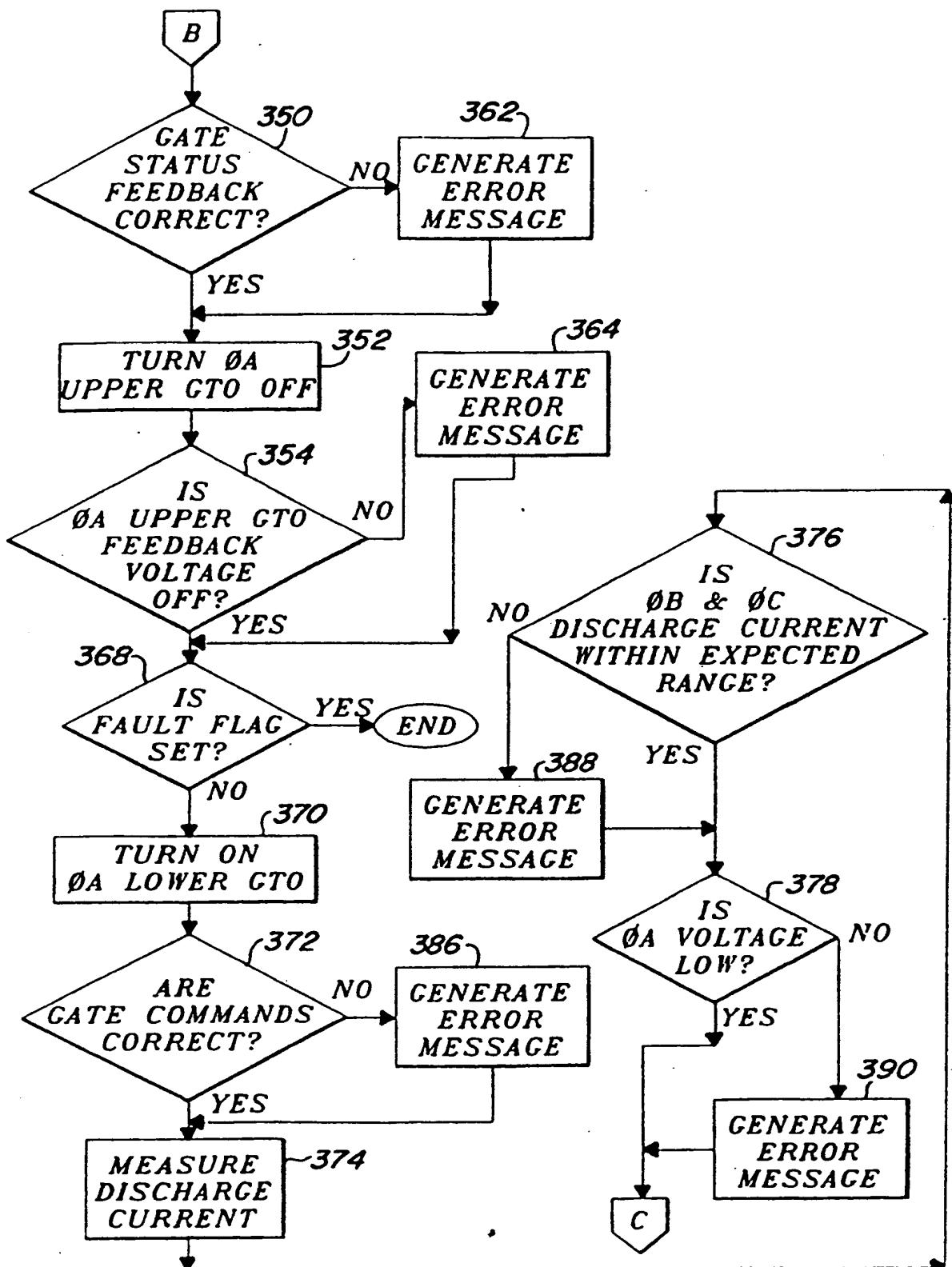


Fig. 5c

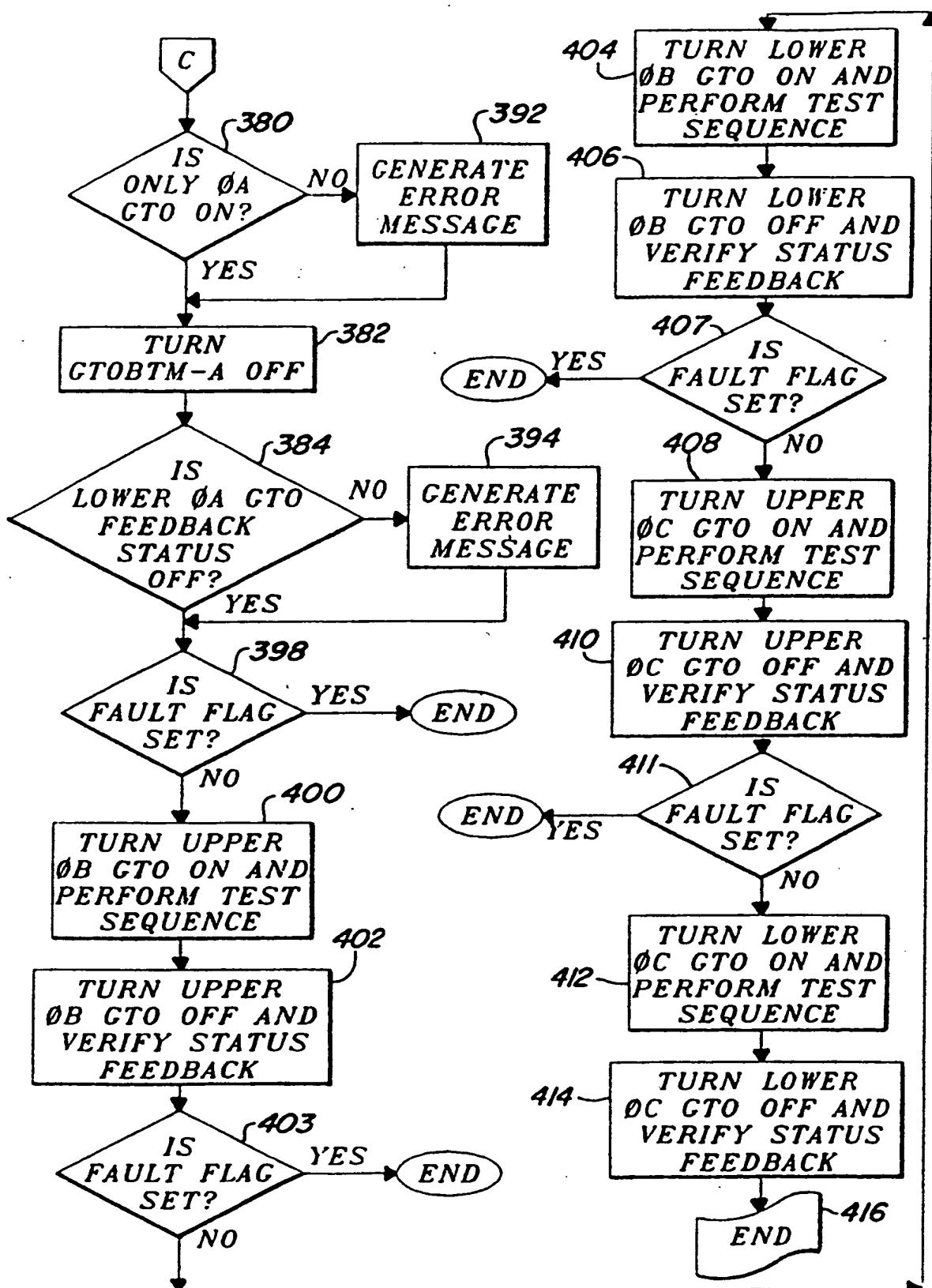


Fig. 5d

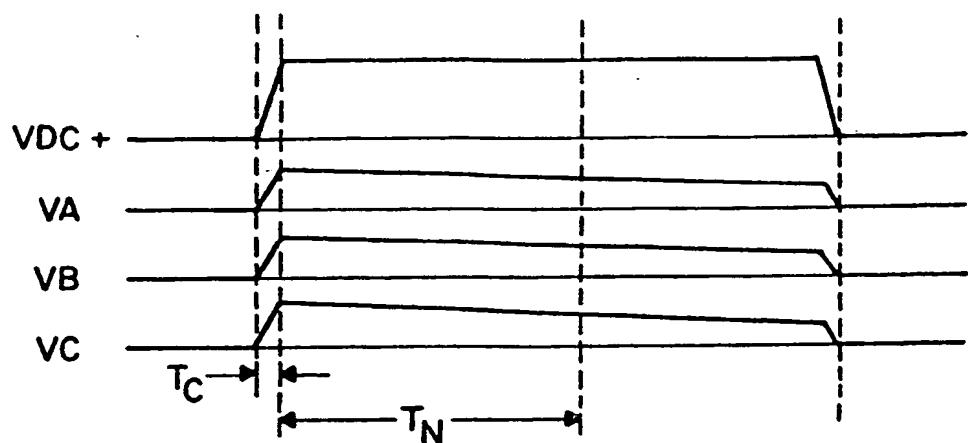


Fig. 6

INTERNATIONAL SEARCH REPORT

Intern: 1 Application No
PCT/US 93/10591A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G01R31/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|----------|--|-----------------------|
| A | FR,A,2 409 625 (LICENTIA) 15 June 1979 --- | |
| A | ELEKTROTECHNIK vol. 73, no. 4, April 1991, WURZBURG, DE pages 62 - 70 XP000227651 BROSCH 'Falsch ist rasch gemessen' --- | |
| A | IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS vol. IA-20, no. 6, November 1984, NEW-YORK, US pages 1490 - 1496 MURTY ET AL. 'Fault diagnosis in three-phase thyristor converters using microprocessor' ----- | |

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

* Special categories of cited documents :

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- *'P' document published prior to the international filing date but later than the priority date claimed

- *'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

7 March 1994

Date of mailing of the international search report

15.03.94

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Hoornaert, W

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern: J Application No

PCT/US 93/10591

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|--|------------------|-------------------------|------------------|
| FR-A-2409625 | 15-06-79 | BE-A- | 872056 16-03-79 |